Analog Readout Circuitry for Wide-Dynamic-Range CMOS image sensors

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Abstract

This paper describes the readout circuitry of a SVGA wide-dynamic-range (>90dB) CMOS image sensor, which is the first of its class to operate at 60 frame/s. Lateral-overflow capacitor CMOS image sensors [1,2] require two images per frame as well as low noise and highly linear circuits. To achieve these specs, high-output impedance pixel current sources with smooth start-up and a 36MHz segmented line memory were implemented. Supporting blocks like the voltage regulators and output amplifier are described too. The chip was made in a 2P3M CIS 0.18μm process.

Signal Flow

Although the fundamental operation of this type of wide dynamic range sensor had been previously published [1,2]; the readout circuitry was still left to be explained. The basic signal flow has not changed: pixel offset (N) and offset+signal (NS) are sampled in a line memory to then flow through a common bus up to a differential amplifier, which subtracts N from NS to make a single ended output.

The S1 (low-light) and S2 (high-light) signals are processed in parallel so the readout circuitry is twice that of a regular CMOS sensor. Both the top and bottom of the pixel array are used to place these circuits (figure 1).

Pixel Biasing

The column current source that biases the pixels uses a cascode in order to increase the pixel linearity. A buffer is needed to drive the 820 gates (figure 2) of the cascode transistors. An original amplifier using common-mode feed-forward was used to speed up the turn-on process (figure 3).

The pixel line and sampling capacitor reset voltage is chosen so as to allow a smooth start-up. On start-up, the line voltage prevents the pixel buffer from turning on and so the capacitor gets linearly discharged until current starts to flow progressively through the pixels.

This start-up approach is very gentle on the voltage supply and prevents fixed-pattern noise. The current sources for the S1 and S2 images have been made independent of each other in order to improve circuit symmetry.

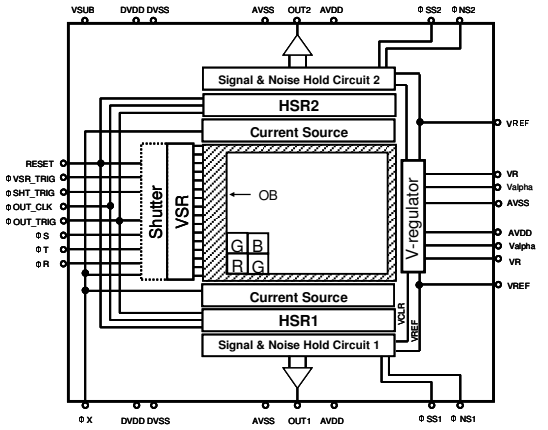

Figure 1, block diagram and pinout

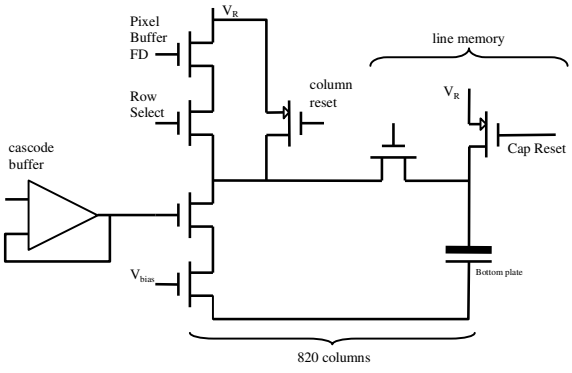

Figure 2, pixel current source

Line Memory

In order to reduce the effects of the common output bus, the capacitors are grouped in "segments" which are connected to the main bus through a switch (figure 5). This reduces dramatically the parasitic capacitance due to the capacitor switches and the lines connecting them to the output bus.

Dividing the image into segments usually causes fixed pattern noise making either each block distinguishable from the other or, in the most benign case, it produces artefacts (like vertical lines) around the segment swap. These effects are prevented by swapping the segments during the reset part of the output (figure 4) and minimizing crosstalk.

As a passive analog circuit, the line memory requires careful attention to layout parasitics and device sensitivities. All digital lines are symmetric in respect to the N-NS signals and the whole layout is designed to match the N and NS paths. Many other cross-talk counter measurements were also taken in the capacitor and segment layout.

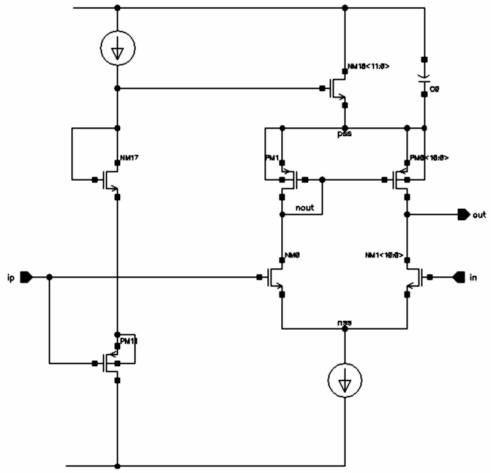

Figure 3, pixel current source, cascode buffer

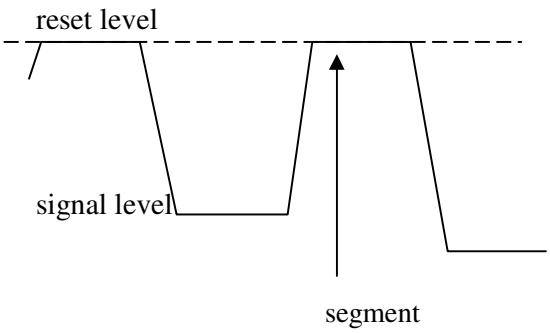

Figure 4, Segment change timing

Ground Layout

In order to avoid horizontal shading (figure 6) due to the pixel biasing, all ground lines from the pixel current sources are collected into a metal funnel whose voltage drop does not cause shading. This avoids the use of dynamic current mirrors [3] and low ρ metal layers.

As this funnel is laid out across the line memory up to the AVSS pin, the placement of the readout circuits had to be changed (figure 1) to reduce the risk of noise coupling. The new order takes into account that the noisiest element (the horizontal scanner) and the most sensible one (the pixel biasing) do not operate at the same time (figure 7).

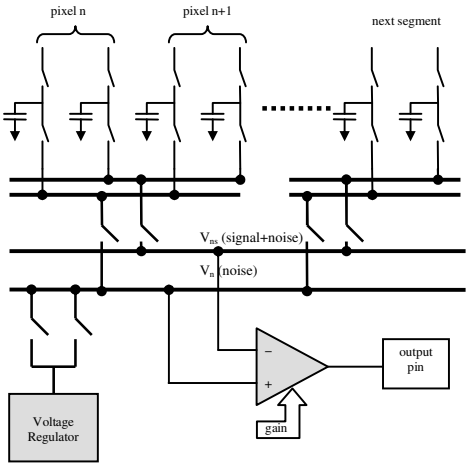

Figure 5, segmented line memory

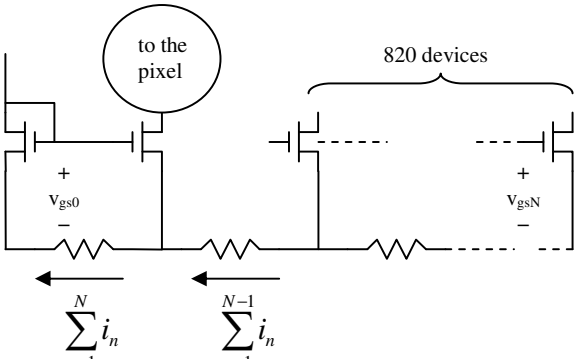

Figure 6 IR drops cause shading in the image

Voltage Regulators

The pixel voltage source is generated on the chip using a low drop out regulator (see figure 8). The line memory bus is reset using another regulator which is made of a simple buffer (figure 9). These regulators track AVDD to guarantee that there is enough headroom to operate the switches adequately.

Differential Amplifier

As the S1 and S2 images use different gains, a PGA (Programmable Gain Amplifier) was used. The amplifier is divided into three stages (figure 10): input buffer, current-mode gain stage and output buffer.
The PGA follows a fully differential architecture [4] for all the inner stages.

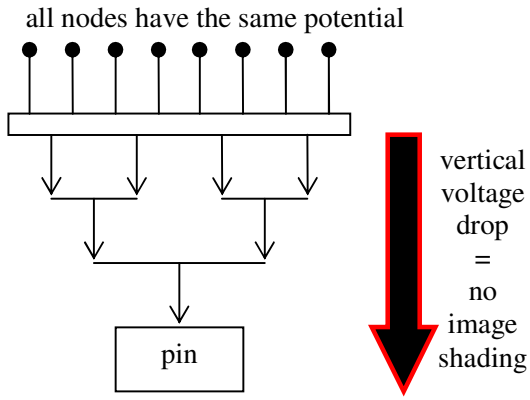

Figure 7, funnel layout

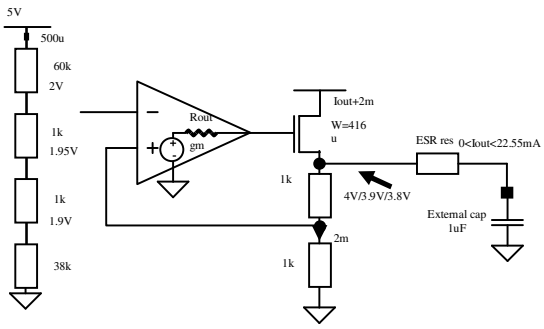

Figure 8, LDO Regulator

Results

This new implementation of the line memory results in a much higher data rate while reducing random and fixed pattern noise. Ghost images and shading due to saturated pixels have also been eliminated (figure 13) thanks to the amplifier-driven cascoded current source with funnel-shaped ground. Pixel linearity, too, is improved (figure 12) by it. On-chip voltage regulators and supply decoupling reduce fixed pattern noise and the use of a differential amplifier rather than two separate buffers highly increases the CDS effectiveness.

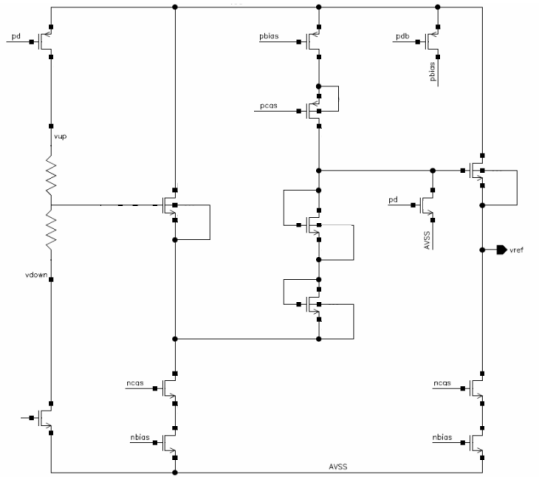

Figure 9, output bus reset voltage buffer

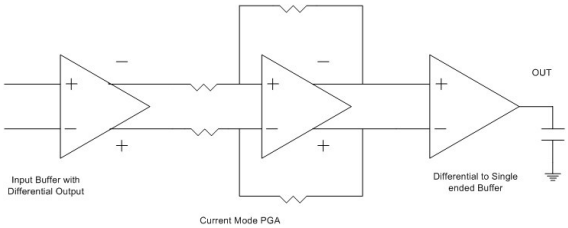

Figure 10, PGA block diagram

References

[1] S. Sugawa et al., 2005 ISSCC Dig. Tech. Papers, pp.352-353, 2005

[2] N. Akahane et al., IEEE J. Solid-State Circuits, vol.41, no.4, pp.851-858, 2006

[3] C. Toumazou et al. "*Analogue IC design: the current-mode approach*", chapter 7. ISBN-13: 978-0863412974

[4] Duque-Carrillo, J.F. et al., IEEE Trans. Electron Devices, vol.42, no.3, pp.190-192, 1995

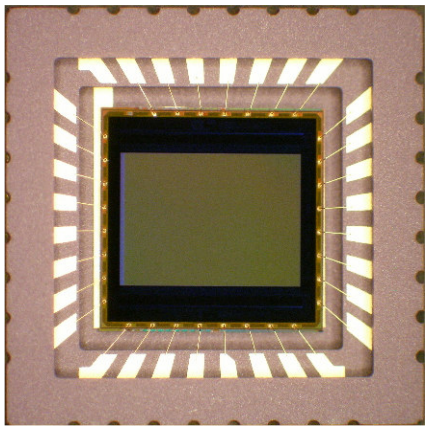

Figure 11, packaged chip

Table 1

Technology	2P3M CIS 0.18µm	
AVDD/DVDD	5	V
Effective pixels	800×600	
pixel pitch	5.6	µm
Frame rate	60	FPS
Pixel rate	36	MHz
Sensitivity	5.7	V/lux-s
Saturation voltage for S1 and S2	1.2	V
Dynamic range	93	dB
PRNU	0.8	%

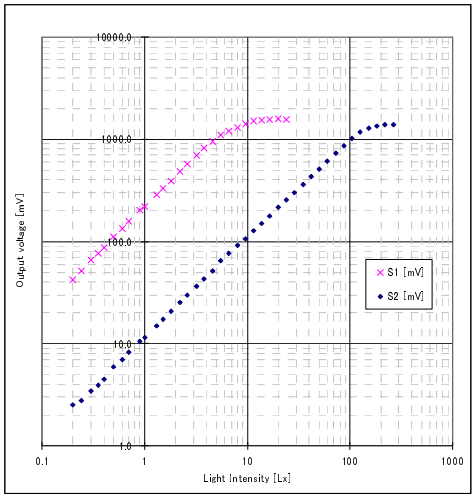

Figure 12, output voltage vs light

Figure 13, image sample